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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,474	08/01/2005	Matthias Muth	DE 020146	6116

24738 7590 04/10/2008

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ART UNIT	PAPER NUMBER
2154	

MAIL DATE	DELIVERY MODE
04/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/517,474	MUTH, MATTHIAS	
	Examiner	Art Unit	
	ASHOK B. PATEL	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *7-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are subject to examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1, 3, 4, and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Referring to claims 1 and 4,

Claims 1 and 4 recite the following phrase: in which all the nodes (20, 22, 24, 26, 28) and/or all the users (30, 32, 34, 36, 38) of the system (100) are addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the system (100) is changed over from subnetwork operation (T) to full network operation (G) if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δtk) of definable or settable length.

Examiner can not understand **how**, "all the nodes (20, 22, 24, 26, 28) of the system (100) are addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the system (100) is changed over from

subnetwork operation (T) to full network operation (G) if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δtk) of definable or settable length", while the nodes as depicted in the drawings as being the "DOTS", possibly showing the "connection" along with no description of it provided in the written specification?

Referring to claims 3 and 6,

Please refer to claims 1 and 4 above for Examiner's questions as these claims recite "at least one of the nodes (20, 24, 26)."

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-15 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. 10/517, 246. Although the conflicting claims are not identical, they are not patentably distinct from each other because the it is the signal level pattern that is detected upon in both set of claims to change over from subnetwork operation to full network operation.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Referring to claims 1, 3, 4, 7, 8, 9, 12 13 and 15,

These claims use of slashes symbol between descriptive elements in the claims renders the scope and meaning of the claims unclear, as slashes could be construed to

mean “and”, “or” or both “and” and “or”. Examiner interprets this as being “or”.

Referring to claims 1 and 4,

Claims 1 and 4 recite “characterized in that the system (100) is changed over from subnetwork operation (T) to full network operation (G) if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δtk) of definable or settable length.”

Examiner does not understand how “a period (Δt)” which is greater than a critical period (Δtk) of definable or settable length? To Examiner, if “a critical period (Δtk) of definable or settable length” is how definable without any units of measurement?

If it is definable, just as it is recited in the claim, then how it establishes it’s relativity with “a period (Δt) which is greater than a critical period (Δtk)?

In these claims “a critical period (Δtk) of definable or settable length” is called definable, however, it represents complete vagueness of relevancy not only to itself but also to the other relevant time period (Δt), please advise.

Claims 1 and 4 recite the following phrase: in which all the nodes (20, 22, 24, 26, 28) and/or all the users (30, 32, 34, 36, 38) of the system (100) are addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the system (100) is changed over from subnetwork operation (T) to full network operation (G) if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δtk) of definable or settable length.

Examiner can not understand how, "all the nodes (20, 22, 24, 26, 28) of the system (100) are addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the system (100) is changed over from subnetwork operation (T) to full network operation (G) if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δtk) of definable or settable length", while the nodes as depicted in the drawings as being the "DOTS", possibly showing the "connection" along with no description of it provided in the written specification?

Referring to claims 2, 3, 5 and 6,

Claims 2 and 5 recite "characterized in that the critical period (Δtk) is selected to be greater than the interval (Δtd) between the individual messages or data packets of the data traffic on the system (100)."

As these claims depend on claims 1 and 4 respectively, these claims inherits the subject matter of independent claims upon which they depend, Base on that rationale, Examiner does not understand how "a critical period (Δtk) of definable or settable length" would become " selectable" all of a sudden in these claims?

To Examiner, it is not clear whether "(Δtd)" is same for "between the individual messages and data packets of the data traffic?

And, if (Δtk) is definable, just as it is recited in the claim, then how it establishes it's relativity with "a period (Δtd) which is shorter than a critical period (Δtk)?

In these claims "a critical period (Δtk) of definable or settable length" is called definable or selectable , however, it represents complete vagueness of relevancy not only to itself but also to the other relevant time period (Δt), please advise.

The same vagueness in the claim is applicable to claims 3 and 5 as they not only depend on claims 2 and 5, but also reiterate "(Δtk)."

Examiner interprets these claims wherein the signal level time period (Δt), is somehow distinguishable, such that the bus nodes or users recognize this signal as being to go for full network operation from subnetwork operation.

Referring to claims 7-15,

These claims are in such an improper form and language leading only towards the vagueness of the subject matter. Examiner has made the best effort to address the claim limitations in the following claim rejection.

Claim Objections

8. Referring to claims 7-15,

Claims 7-14 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only, or, cannot depend from any other multiple dependent claim See MPEP § 608.01(n). Accordingly, the claim 7-14 has been further treated on the merits accordingly. Please advise.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Lenz (US 6, 484, 233 B1)

Referring to claim 1,

Lenz teaches a method for changing over a serially networked system (100), in particular a serial databus system, from subnetwork operation (T), in which at least one node (22, 28) and/or at least one user (32, 38) of the system (100) (ABSTRACT: The invention relates to a transmitting device and a bus system for the serial data transfer of binary data between at least two communication stations, which are coupled to one another via an individual bus line.") is in a state of reduced current consumption and is not addressed and/or not activated by the signal level (40, 42, 44) of the data traffic on the system (100), to full network operation (G), in which all the nodes (20, 22, 24, 26, 28) and/or all the users (30, 32, 34, 36, 38) of the system (100) are addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the system (100) is changed over from subnetwork operation (T) to

full network operation (G) (col. 4, line 14-26, “In a special operating mode, the so-called wake-up mode, a so-called wake-up signal can thus be impressed on the bus line. This wake-up signal has a distinctly increased amplitude compared with the normal signal, in accordance with the amplification. This wake-up signal of a master unit wakes up all the network nodes on the bus system which were previously in the so-called sleep mode and then selectively activates them or controls them such that they attain the sleep mode again. In an advantageous manner the average current consumption of a bus system is considerably reduced by means of the wake-up mode, since all, sleeping, network nodes which are not addressed during a bus transfer remain in the current-saving sleep mode.") if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δtk) of definable or settable length (col. 9, line 52-col. 10, line 3, “The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep

mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ")

Referring to claim 2,

Lenz teaches a method as claimed in claim 1, characterized in that the critical period (Δtk) is selected to be greater than the interval (Δtd) between the individual messages or data packets of the data truffle on the system (100) (col. 9, line 52-col. 10, line 3, "The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ").

Referring to claim 3,

Lenz teaches a method as claimed in claim 1 or 2, characterized in that messages or data packets are sent by at least one of the nodes (20, 24, 26) and/or users (30, 34, 36) participating in subnetwork operation (T) at cyclic intervals which are smaller than the critical period (Δtk) (col. 9, line 52-col. 10, line 3, "The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ").

Referring to claim 4,

Lenz teaches a serially networked system (100) (ABSTRACT: The invention relates to a transmitting device and a bus system for the serial data transfer of binary data between at least two communication stations, which are coupled to one another via an individual bus line."), which is intended to be changed over from subnetwork

operation (T), in which at least one node (22, 28) and/or at least one user (32, 38) of the system (100) is in a state of reduced current consumption and cannot be addressed and/or activated by the signal level (40, 42, 44) of the data traffic on the system (100), to full network operation (G), in which all the nodes (20, 22, 24, 26, 28) and/or all the users (30, 32, 34, 36, 38) of the system (100) may be addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100) (col. 4, line 14-26, “In a special operating mode, the so-called wake-up mode, a so-called wake-up signal can thus be impressed on the bus line. This wake-up signal has a distinctly increased amplitude compared with the normal signal, in accordance with the amplification. This wake-up signal of a master unit wakes up all the network nodes on the bus system which were previously in the so-called sleep mode and then selectively activates them or controls them such that they attain the sleep mode again. In an advantageous manner the average current consumption of a bus system is considerably reduced by means of the wake-up mode, since all, sleeping, network nodes which are not addressed during a bus transfer remain in the current-saving sleep mode."), characterized in that the changeover from subnetwork operation (I) to full network operation ((3) takes place if the system (100) is in the signal rest level (50) state and/or an unchanged signal level state for a period (At) which is greater than a critical period (Ate) of definable or settable length (col. 9, line 52-col. 10, line 3, “The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line

1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ").

Referring to claim 5,

Lenz teaches a system as claimed in claim 4, characterized in that the critical period (Δtk) is greater than the interval (Δtd) between the individual messages or data packets of the data traffic on the system (100) (col. 9, line 52-col. 10, line 3, "The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2

which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ").

Referring to claim 6,

Lenz teaches a system as claimed in claim 4 or 5, characterized in that at least one of the nodes (20, 24, 26) and/or users (30, 34, 36) participating in subnetwork operation (T) sends messages or data packets at cyclic intervals which are smaller than the critical period (Δtk) (col. 9, line 52-col. 10, line 3, "The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up

voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ").

Referring to claim 7,

Lenz teaches a system as claimed in at least one of claims 4 to 6, characterized in that the system (100) comprises at least one serial databus (10), in particular at least one C [ontroller]A[rea]N[etwork] bus. (col. 4, line 66-col. 5, line 4, "The invention is particularly suitable in the automotive arts, i.e., in so-called CAN on-board electrical systems. In this case, a microprocessor controls the data transfer via the single-wire bus via an internal bus and a so-called CAN module, which contains the corresponding CAN protocol, via the transceiver circuit.")

Referring to claim 8,

Lenz teaches a system as claimed in at least one of claims 4 to 7, characterized in that the user (30, 32, 34, 36, 3g) takes the form of at least one system chip unit (80), in particular at least one system chip unit, and/or at least one microcontroller (90) unit provided for carrying out at least one application. (col. 5, line 66-col. 6, line 5, "Furthermore, the network node 2 has a microprocessor 6, an I/O device 7 and also a memory unit 8. The various units are each connected to the internal bus 4. It is particularly advantageous, as illustrated in FIG. 1, if the elements 3 to 8 of a network node 2 are monolithically integrated on a single semiconductor chip. This is advantageous in particular for reasons of cost on account of the smaller space requirement.")

Referring to claim 9,

Lenz teaches a transceiver unit (84), in particular for carrying out a method as claimed in at least one of claims I to 3 and/or in particular associated with at least one system (I00) as claimed in at least one of claims 4 to 8, characterized in that the transceiver unit (84) is connected to at least one serial databus (10), in particular to at least one C[ontroller]A[rea]N[etwork] bus, and is in communication (982) with at least one microeontroller unit (90) which is provided to carry out at least one application (col. 4, line 66-col. 5, line 4, "The invention is particularly suitable in the automotive arts, i.e., in so-called CAN on-board electrical systems. In this case, a microprocessor controls the data transfer via the single-wire bus via an internal bus and a so-called CAN module, which contains the corresponding CAN protocol, via the transceiver circuit.")

Referring to claim 10,

Lenz teaches a transceiver unit as claimed in claim 9, characterized by at least one control logic associated with the transceiver unit (84) and/or implemented in the transceiver unit (84) (Fig. 4, col. 8, line 12-21).

Referring to claim 11,

Lenz teaches a voltage regulator (86) which is connected to at least one battery unit (70) (Fig. 1, elements 8a and 8b, col. 6, line 6-9, "Furthermore, a voltage supply line 8a for the voltage supply is provided. The voltage supply line 8a is connected to a voltage regulating module 8b typically provided in the communication device 2."), and which is in communication (886) with at least one transceiver unit (84), in particular as claimed in claim 9 or 10, which voltage regulator is intended to supply a voltage to at least one microcontroller unit (90), provided to execute at least one application, in the

event of detection, by the transceiver unit (84), of at least one def'med, in particular continuous and/or in particular symmetrical signal level pattern in at least one incoming message associated with at least one application and occurring on at least one serial databus (10), in particular on at least one C[ontroller]A[rea]N[etwork] bus.(col. 6, line 9-17, "Consequently, the voltage regulating module 8b draws its supply voltage via the voltage supply line 8a and provides the feeding voltage for all the above-mentioned modules of the network node 2. Since the requirements of high currents and high voltages have to be fulfilled both by the transceiver 3 and by the voltage regulating module 8b, it is advantageous for these modules, in particular, to be monolithically integrated on a single semiconductor chip.")

Referring to claim 12,

Lenz teaches a chip unit (80), in particular a system chip unit, for addressing and/or activating at least one microcontroller unit (90) which is provided to carry out at least one application and which is associated with at least one serial databus (10), in particular at least one C[ontroller]A[rea]N[etwork] bus; characterized by - at least one transceiver unit (84) as claimed in claim 9 or I0, and - at least one voltage regulator (g6) as claimed in claim 11. (col. 4, line 66-col. 5, line 4, "The invention is particularly suitable in the automotive arts, i.e., in so-called CAN on-board electrical systems. In this case, a microprocessor controls the data transfer via the single-wire bus via an internal bus and a so-called CAN module, which contains the corresponding CAN protocol, via the transceiver circuit.", col. 5, line 66-col. 6, line 5, "Furthermore, the network node 2 has a microprocessor 6, an I/O device 7 and also a memory unit 8. The

various units are each connected to the internal bus 4. It is particularly advantageous, as illustrated in FIG. 1, if the elements 3 to 8 of a network node 2 are monolithically integrated on a single semiconductor chip. This is advantageous in particular for reasons of cost on account of the smaller space requirement.")

Referring to claim 13,

Lenz teaches a microcontroller unit (90) provided to carry out at least one application and associated with at least one serial data bus (10), in particular at least one C[ontroller]A[rea]N[etwork] bus, which microcontroller unit is to be supplied with a voltage only if at least one defined, in particular continuous and/or in partioular symmetrical signal level pattern is detected in at least one incoming message associated with at least one application and occurring on the databus (10), by at least one transceiver unit (84), in particular as claimed in claim 9 or 10. (col. 4, line 66-col. 5, line 4, "The invention is particularly suitable in the automotive arts, i.e., in so-called CAN on-board electrical systems. In this case, a microprocessor controls the data transfer via the single-wire bus via an internal bus and a so-called CAN module, which contains the corresponding CAN protocol, via the transceiver circuit.", col. 5, line 66-col. 6, line 5, "Furthermore, the network node 2 has a microprocessor 6, an I/O device 7 and also a memory unit 8. The various units are each connected to the internal bus 4. It is particularly advantageous, as illustrated in FIG. 1, if the elements 3 to 8 of a network node 2 are monolithically integrated on a single semiconductor chip. This is advantageous in particular for reasons of cost on account of the smaller space requirement." col. 4, line 14-26, "In a special operating mode, the so-called wake-up

mode, a so-called wake-up signal can thus be impressed on the bus line. This wake-up signal has a distinctly increased amplitude compared with the normal signal, in accordance with the amplification. This wake-up signal of a master unit wakes up all the network nodes on the bus system which were previously in the so-called sleep mode and then selectively activates them or controls them such that they attain the sleep mode again. In an advantageous manner the average current consumption of a bus system is considerably reduced by means of the wake-up mode, since all, sleeping, network nodes which are not addressed during a bus transfer remain in the current-saving sleep mode."), characterized in that the changeover from subnetwork operation (I) to full network operation ((3) takes place if the system (100) is in the signal rest level (50) state and/or an unchanged signal level state for a period (At) which is greater than a critical period (Ate) of definable or settable length (col. 9, line 52-col. 10, line 3, “The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1,

during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ")

Referring to claim 14,

Lenz teaches a microcontroller unit (90) as claimed in claim 13, characterized in that the microcontroller unit (90) may be activated by the transceiver unit (84) (col. 4, line 66-col. 5, line 4, “The invention is particularly suitable in the automotive arts, i.e., in so-called CAN on-board electrical systems. In this case, a microprocessor controls the data transfer via the single-wire bus via an internal bus and a so-called CAN module, which contains the corresponding CAN protocol, via the transceiver circuit.”, col. 5, line 66-col. 6, line 5, “Furthermore, the network node 2 has a microprocessor 6, an I/O device 7 and also a memory unit 8. The various units are each connected to the internal bus 4. It is particularly advantageous, as illustrated in FIG. 1, if the elements 3 to 8 of a network node 2 are monolithically integrated on a single semiconductor chip. This is advantageous in particular for reasons of cost on account of the smaller space requirement.” col. 4, line 14-26, “In a special operating mode, the so-called wake-up mode, a so-called wake-up signal can thus be impressed on the bus line. This wake-up signal has a distinctly increased amplitude compared with the normal signal, in accordance with the amplification. This wake-up signal of a master unit wakes up all the network nodes on the bus system which were previously in the so-called sleep mode and then selectively activates them or controls them such that they attain the sleep mode again. In an advantageous manner the average current consumption of a

bus system is considerably reduced by means of the wake-up mode, since all, sleeping, network nodes which are not addressed during a bus transfer remain in the current-saving sleep mode."), characterized in that the changeover from subnetwork operation (I) to full network operation ((3) takes place if the system (100) is in the signal rest level (50) state and/or an unchanged signal level state for a period (At) which is greater than a critical period (Ate) of definable or settable length (col. 9, line 52-col. 10, line 3, "The circuit for edge form setting 9 is activated in the wake-up mode. At the same time, the gain of the output signal 21 is increased by corresponding control of the feedback path 35 of the amplifier device 33. As a result, a so-called wake-up signal is impressed on the bus line 1. This wake-up signal has a considerably increased amplitude compared with the normal signal. The wake-up signal of a master unit "wakes up" all the network nodes 2 on the bus system and then selectively activates them or switches them back to the sleep mode. The average current consumption of a bus system is considerably reduced by means of this wake-up mode, since all the "sleeping" network nodes 2 which are not addressed during a bus transfer remain in the sleep mode. The receiving device 43, 44, 10b consequently forwards a data packet 42, arriving from the bus 1, during the sleep mode to the microcontroller 6 connected downstream only when it has identified the wake-up voltage level, which is distinctly higher than the normal level, for a defined minimum period of time. ").

Referring to claim 15,

Claim 15 is a claim to the use of a method as claimed in at least one of claims 1 to 3. Therefore claim 15 is rejected for the reasons set forth for claims 1 to 3.

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 6:30 am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan A. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ashok B. Patel/

Examiner, Art Unit 2154